**Processor Design**

**Lab Session – 1**

**Selection Criteria**

The microprocessor we have chosen for the

Baseline Processor

* ARM Amber
* MIPS 32
* OpenRISC
* MIPS 16/ Something in VHDL

Marks out of 5

Documentation

Last Update of the project

Source Code – Verilog

Code Clarity

ISA

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
|  | AMBER ARM  23 | AMBER ARM  25 | MIPS Educational 16 bits | OpenRISC | Some in VHDL |
| Documentation |  |  |  |  |  |
| Last Update |  |  |  |  |  |
| Source Code | Verilog | Verilog | Verilog |  |  |
| Code Clarity |  |  |  |  |  |
| Complexity |  |  |  |  |  |
| ISA |  |  |  |  |  |
| # Stages | 3 stages | 5 stages | 5 stages | 5 stages | 5 stages |
| Memory hierarchy |  |  |  |  |  |