**Processor Design**

**Lab Session – 1**

**Selection Criteria**

The microprocessor we have chosen for the

Baseline Processor

* ARM Amber
* MIPS 32
* OpenRISC
* MIPS 16/ Something in VHDL

Marks out of 5

Documentation

Last Update of the project

Source Code – Verilog

Code Clarity

ISA

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
|  | Doc | Last Updat | Soiurce | Code Clarity | ISA |
| ARM 3 | 2 |  |  |  |  |
|  | Kajkjfs |  |  |  |  |
| ARM 5 |  |  |  |  |  |
| MIPS | 4 |  |  |  |  |
|  | nvkdsnk |  |  |  |  |
| OpenRISC |  |  |  |  |  |