Processor Design

Lab Session – 1 Beatriz Aguilar Gallo Rajagopal Hariharan

**Selection Criteria**

The microprocessor we have chosen for the

Marks out of 5

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
|  | AMBER ARM  23 | AMBER ARM  25 | MIPS Educational 16 bits | OpenRISC | Some in VHDL |
| Doc Quality | 5 |  | 2 |  |  |
| Reason | The project it is really well documented. There is a schematic of the processor and all the stages are explained in detail. |  | The documentation is in Chinese. There is a schematic but impossible to understand the explanations. |  |  |
| Last Update | May,20,2013 |  | Aug 18, 2013 |  |  |
| Status | Stable |  | Stable |  |  |
| Source Code | Verilog |  | Verilog |  |  |
| Code Clarity | 5 |  | 4 |  |  |
| Reason | It is well commented. The indentation of the code is really clean so it is easy follow it. |  | The code is really simple so it is easy to understand but we miss some additional comments. |  |  |
| Complexity | 4 |  | 1 |  |  |
| Reason | The processor is a little bit complex because there are a lot of control signals, but the clarity of the code and the documentation make up for this complexity. |  | It is the simplest processor we found, the principal reason it is that there has no cache. |  |  |
| ISA | ARM |  | MIPS |  |  |
| # Stages | 3 stages |  | 5 stages |  |  |